Charge-coupled devices and applications

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Charge-coupled devices (CCD's) represent a new concept for silicon integrated circuits. This article reviews the basic operation of CCD's, including their basic operating limitations, methods of fabrication, and state-of-the-art experimental results; the various potential applications are then described in more detail.

THE CHARGE COUPLED DEVICE[1,2] (CCD) is a new device concept which was introduced three years ago. It is an analog shift register, and as such has potential application in a variety of areas such as self-scanned image sensors, electronically-variable analog delay lines, matched filters, and autocorrelators. In addition, the simplicity and compactness of CCD's should result in their use as low cost, high capacity digital serial memories. Progress in CCD research has been rapid. Initial announcements told of devices having just eight stages with an efficiency per stage of approximately 99%.[2] In the succeeding years, the length of devices and their transfer efficiencies have increased at the rate of approximately one order of magnitude per year, so that present devices have as many as 500 stages[3] and efficiencies of 99.99%.[4,5] Devices with this type of performance are satisfactory for most of the applications mentioned and it is anticipated that CCD's will soon find their way into marketable products.

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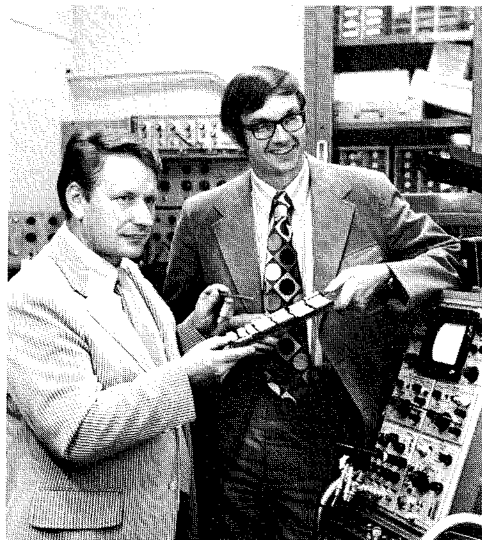

MOS capacitor

Since a CCD is physically just a linear array of closely-spaced MOS (metal-oxide-semiconductor) capacitors, it is important to understand the MOS capacitor and how the surface potential, V_S (the potential at the Si-SiO_2 interface relative to the potential in the bulk of the silicon), depends upon the various parameters involved.

Fig. 1 shows a cross-sectional view of an MOS capacitor with a p-type silicon substrate. When a positive step voltage is applied to the gate of such a structure, the majority carrier, holes, are repelled and respond within the dielectric relaxation time. This results in a depletion region of negatively-charged acceptor states near the surface of the silicon. The applied gate voltage is dropped across the series combination of the oxide and the depletion region in the silicon. Solution of the one-dimensional Poisson's equation subject to the appropriate boundary conditions, and including two-dimensional sheets of charge at the Si-SiO_2 interface due to fixed oxide charge (Q_{SS}) and signal charge represented by minority carriers (Q_{sig}), shows that the surface potential V_S is given by:

$$V_S = V_G' - B\left[\left(1+\frac{2V_G'}{B}\right)^{1/2} - 1\right] \quad (1)$$

where
$V_G' = V_G + (X_{ox}/\varepsilon_{ox})\ (Q_{SS}+Q_{sig})$; V_G is

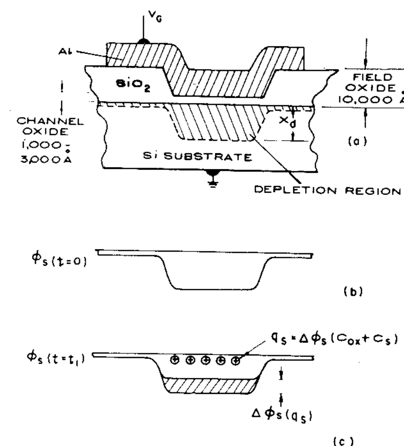

Fig. 1—(a) Cross-sectional view of an MOS capacitor representing element for charge-coupled circuit; (b) Surface potential profile just after application of step voltage V_G; (c) Surface potential profile with charge signal q_s in the potential well.

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received the BSEE and MSEE from Newark College of Engineering in 1955 and 1957, respectively, and the ScD in Engineering from Columbia University in 1965. From June 1955, he has been employed at RCA Laboratories, where after one year as a Research Trainee, he became a Member of the Technical Staff and since that time he has been doing research on new solid-state devices and circuits. Since the spring of 1970, Dr. Kosonocky has been working on the study of performance limitations of CCD's and the development of charge-coupled devices for digital memories and self-scanned image sensors. Dr. Kosonocky received two RCA Laboratories Achievement awards in 1959 and 1963, and was awarded a David Sarnoff Fellowship for the academic year 1958-1959. During 1958-1959 and 1965-1966, Dr. Kosonocky was a lecturer and then Adjunct Professor of Electrical Engineering at Newark College of Engineering, and since 1969 he has been a lecturer at LaSalle College. He has published 24 technical papers, and has been issued 23 U. S. patents. Dr. Kosonocky is a member of Tau Beta Pi, Eta Kappa Nu, Sigma Xi, the American Ordnance Association, and a Senior Member of IEEE. Dr. Kosonocky is also a member of the IEEE Solid State Circuit Committee.

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received the BS in Engineering Science from Pennsylvania State University with distinction in 1961. After four years in the U.S. Navy, he entered Princeton University and received the MA and PhD in Electrical Engineering (Solid State Device Physics) in 1967 and 1970, respectively. His PhD dissertation was an investigation of photo-induced currents and charge transport in polyvinyl-carbazole, an organic polymer. During the summers of 1966 and 1967, Dr. Carnes was employed at the David Sarnoff Research Center doing experimental work with evaporated metallic contacts and DC electroluminescence in strontium titanate. Since September 1969, when he joined the RCA Laboratories staff, Dr. Carnes has studied electrical breakdown, conduction and interface properties of various thin insulating films on silicon, including silicon dioxide, silicon nitride, and aluminum oxide. He is currently involved in the investigation of charge-coupled devices. Dr. Carnes is a member of the American Physical Society, Tau Beta Pi, Phi Kappa Phi, and IEEE.

the applied gate voltage; Q_{SS} is the fixed oxide charge; Q_{sig} is the signal charge of minority carriers (inversion layer charge); $B=qN_A\varepsilon_s X_{ox}^2/\varepsilon_{ox}^2=0.15 (N_A/10^{15}) (X_{ox}/1000Å)^2$; q is the electronic charge in coulombs; N_A is the doping density in acceptors/cm^3; ε_s is the dielectric constant of silicon; ε_{ox} is the dielectric constant of the oxide layer; and X_{ox} is the thickness of the oxide layer. Eq. 1 is a most important one in CCD design.

Just after the step voltage is applied to the gate and in the absence of signal charge Q_{sig} (the introduction of signal charge will be discussed in the next section), the silicon conduction band at the surface is well below the equilibrium Fermi level and electrons, the minority carriers, will tend to gather there. However, it takes a rather long period of time for thermally-generated minority carriers to accumulate in sufficient numbers to return to the system to thermal equilibrium. We have measured thermal relaxation times for MOS capacitors ranging from 1 to 100 seconds in good agreement with the predicted[6] values assuming bulk thermal generation of minority carriers:

$$T=\tau N_A/2n_i \qquad (2)$$

where τ is the minority carrier lifetime; N_A is the doping density; and n_i is the intrinsic carrier concentration (1.45×10^{10}cm^{-3} for silicon).

When minority carriers do accumulate at the surface, they start to create an inversion layer which resides within 100Å of the interface. This negative charge tends to reduce V_S according to Eq. 1. When V_S goes to zero, no more charge can be accumulated or stored in the potential well. The capacitance of the potential well, C_{well}, consists of two capacitances in parallel: the fixed oxide capacitance, $C_{ox}=\varepsilon_{ox}/X_{ox}$, and the capacitance associated with the depletion layer of the silicon, $C_d=(2qN_A\varepsilon_s/V_s)^{1/2}$. Since C_d depends upon V_S, C_{well} is not constant for all values of V_S and, therefore, the concept of a potential well capacitance has limited usefulness. However, for large enough values of V_S, $C_d \ll C_{ox}$ and $C_{well} \approx C_{ox}$. For V_S values greater than $200B$, C_d will be less than 10% of C_{ox}, and C_{well} is essentially constant at C_{ox}.

Thus, the following fluid model of the MOS capacitor emerges: a potential

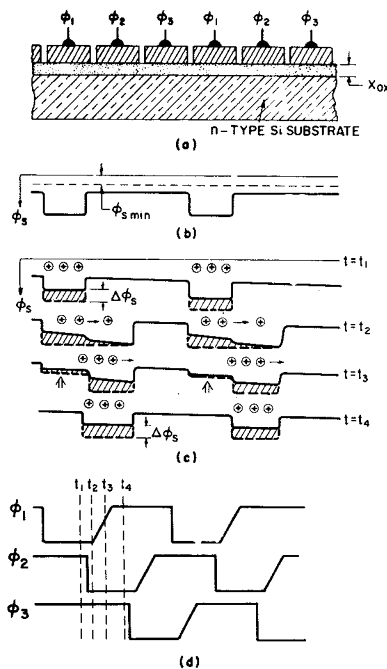

Fig. 2—Operation of a 3-phase charge coupled shift register: (a) Cross section of the structure along the channel oxide; (b) Surface potential profile for $\phi_1=-V$, $\phi_2=0$, $\phi_3=0$ forming a potential well under the phase-1 electrode; (c) Transfer of charge from the potential wells under the phase-1 electrode to the potential wells under the phase-2 electrode illustrated by the profiles of surface potential at times shown in (d); (d) Waveforms of the phase voltages.

well for minority carriers can be created by applying a step voltage to the gate and this well will take a relatively long period of time to accumulate charge thermally. For times much shorter than this thermal relaxation time, a potential well exists at the surface, and the depth of this well can be altered by changing the gate voltage. When minority carriers are introduced as signal charge in the potential well, they tend to reduce the depth of the well according to Q_{sig}/C_{ox}, so they tend to fill up the well much like fluid in a container.

Basic charge-transfer action

A three-phase CCD is just a line of these MOS capacitors spaced very close together with every third one connected to the same gate, or clock voltage as shown in Fig. 2a. If a higher positive voltage is applied to the ϕ_1 clock line than ϕ_2 and ϕ_3, the surface potential variation along the interface will be similar to Fig. 2b. If the device is illuminated by light, charge will accumulate in these wells. Charge can also be introduced electrically at one end of the line of capacitors from a source diffusion controlled by an input gate. To transfer this charge to the right to the position under the ϕ_2 electrodes, a positive voltage is applied to the ϕ_2 line. The potential well there initially goes deeper than that under a ϕ_1 electrode, which is storing charge, and the charge tends to move over under the ϕ_2 electrodes. Clearly, the capacitors have to be close enough so that the depletion layers overlap strongly, and the surface potential in the gap region is a smooth transiston from the one region to the other. Next, the positive voltage on the ϕ_1 line is removed to a small positive DC level, enough to maintain a small depletion region, increasing the surface potential under the ϕ_1 gates in the process. Now the ϕ_2 wells are deeper, and any charge remaining under ϕ_1 gates spills into the ϕ_2 wells. The charge, at least most of it, now resides one-third of a stage to the right under ϕ_2 gates. The charge is prevented from moving to the left by the barrier under the ϕ_3 gates. A similar process moves it from ϕ_2 to ϕ_3 and then from ϕ_3 to ϕ_1. After one complete cycle of a given clock voltage, the charge pattern moves one stage (three gates) to the right. No significant amount of thermal charge accumulates in a particular well because it is continually being swept out by the charge transfer action.

The charge being transferred is eventually transferred into a reversed-biased drain diffusion and from there it is returned to the substrate. The charging current required once each cycle to maintain the drain diffusion as a fixed potential can be measured to determine the signal magnitude (current-sensing) or a re-settable floating diffusion which controls the potential of a MOSFET gate can be employed (voltage-sensing).[7]

The operation of the input and the output circuits for CCD's are described in more depth later in this paper (see *Experimental Results*). One can visualize a CCD shift register as a multigate MOSFET in which the charge signal is moved as charge packets from the source diffusion to the drain diffusion under the control of phase clock voltages applied to the gates.

Limitations on speed and efficiency

Clearly, 100% of the charge cannot move instantaneously from one poten-

tial to another. Also, some of the charge gets trapped in fast interface states at each site and cannot move at all. Therefore, in a given clock period not quite all of the charge is transferred from one well to the next. The fraction of the total that is transferred (per gate) is called the transfer efficiency, η .The fraction left behind is the loss per transfer, denoted ε, so that $\eta+\varepsilon=1$. Because η determines how many transfers can be made before the signal is seriously distorted and delayed, it is a very important figure of merit for a CCD. If a single charge pulse with initial amplitude P_o is transferred down a CCD register, after n transfers the amplitude P_n will be:

$$P_n=P_o\eta^n\cong P_o(1-n\varepsilon) \quad \text{(for small } \varepsilon) \tag{3}$$

When $n\varepsilon=1$, the original pulse is completely lost and distributed among several trailing pulses. Clearly, ε must be very small if a large number of transfers are required. If we allow an $n\varepsilon$ product of 0.1, an overall loss of 10%, then a 3ϕ, 330 stage shift register requires $\varepsilon\leq10^{-4}$, or a transfer efficiency of 99.99%.

The maximum achievable value for η is limited by how fast the free charge can transfer between adjacent gates[8] and how much of the charge gets trapped at every gate location by fast interface states.[9]

Three separate mechanisms cause the free charge to move from one well to another: self-induced drift, thermal diffusion, and fringing field drift. Self-induced drift[10] is a charge-repulsion effect which is only important at large signal charge densities ($\geq10^{10}$ charges/cm^2) and is not particularly significant for achieving very high transfer efficiencies. Thermal diffusion results in an exponential decay of charge under the transferring electrode[11] with time constant

$$\tau_{th}=L^2/2.5D \tag{4}$$

where L is the center-to-center electrode spacing; and D is the diffusion constant.

By means of thermal diffusion alone, 99.99% of the charge is transferred each cycle at frequencies f_4 (in Hz) given approximately by:

$$f_4\,(\textit{thermal diffusion})=5.6\times10^7/L^2 \tag{5}$$

assuming $D=6.75$; L is center-to-center spacing measured in μm. Fringing field drift can help to speed up the charge transfer process considerably. The fringing field is the electric field along the direction of charge propagation at the $Si\text{-}SiO_2$ interface. This field will vary with distance along the gate with the minimum occurring at the center of the transferring gate. The magnitude of the fringing field increases with increasing oxide thickness and gate voltage and decreases with increasing gate length and doping density.[12] The effect of the fringing field upon charge transfer is difficult to assess analytically. A computer simulation of the transfer process under influence of strong fringing fields has indicated that the charge remaining under the transferring electrode still decays exponentially with decay time.

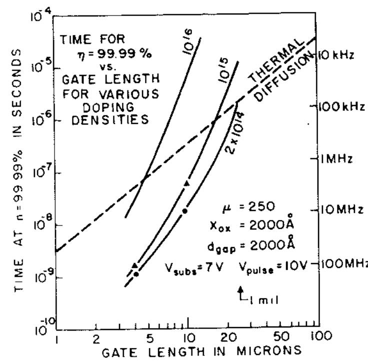

Fig. 3—Time required to achieve η = 99.99% *vs.* gate length for various doping levels The thermal diffusion line is the maximum time required in any case.

$$\tau_f=\frac{L^3}{20\mu X_{ox}V}\left[\frac{5Xd/L+1}{5Xd/L}\right]^4 \tag{6}$$

where V is the clock-pulse voltage; and X_d is the depletion layer thickness at the center of the transferring electrode.

Fig. 3 shows the time required to reach $\eta=99.99\%$ as a function of gate length for various substrate doping densities. According to these calculations for a p-channel CCD, $\eta=99.99\%$ is possible at clock frequency of 10 MHz with gate length $L=7$ μm and substrate doping of $10^{15}cm^{-3}$. This assumes that trapping effects are negligible.

Charges can be lost from the signal into fast interface states because, while the filling rate of these states is proportional to the number of free carriers, the empty rate depends only upon the energy level of the interface state. Thus, even though a roughly equal amount of time is available for filling as for emptying, many of the interface states can fill much faster than they can empty, and thus retain some of the signal charge and release it into trailing signal packets.[9] This type of loss can be minimized by continually propagating a small zero-level charge or fat zero through the device. This tends to keep the slower states filled so they do not have to be filled by the signal charge. An analytical expression for fractional loss into fast interface states ε_s is given by:

$$\varepsilon_s=\left(\frac{\frac{1}{n_{s,o}}}{\frac{n_s}{n_{s,o}}+1}\right)kTN_{ss}\ln\left(1+\frac{2f}{k_1n_{s,o}}\right) \tag{7}$$

where $n_{s,o}$ is the fat zero carrier density in charges/cm^2; n_s is the signal density in chgs/cm^2; kT is in units of eV (0.026 at room temperature); N_{SS} is the fast state density in states/$(eV-cm^2)$; f is the clock frequency; and k_1 is a constant depending upon the trapping cross-section ($\sim10^{-2}cm^2/sec$).

Eq. 7 implies that, without fat zero, $\varepsilon_s\approx10^{-2}$ for $N_{SS}=10^{11}$ $(cm^2-eV)^{-1}$, and $\varepsilon_s\approx10^{-3}$ for $N_{SS}=10^{10}$ $(cm^2-eV)^{-1}$ at 1-MHz clock frequency. By introducing $n_{s,o}$ equal to approximately 10 to 25% of a full well, ($\sim2\times10^{11}cm^{-2}$), interface state losses can be essentially eliminated. For example, suppose $n_{s,o}=2\times10^{11}$, $n_s=10^{12}$, and $f=10^6$. Then:

$$\varepsilon_s=2.2\times10^{-7} \text{ for } N_{SS}=10^{10}$$
$$2.2\times10^{-6} \text{ for } N_{SS}=10^{11}$$

Methods of fabricating CCD's

Three-phase single-level metal CCD's

The three-phase CCD whose operation was described earlier can be made by standard p-MOS or n-MOS techniques. Only one level of metal is required in addition to source and drain diffusions. The gap between adjacent electrodes presents the major problems.

The gap should be as small as possible to insure good coupling between gates without any bumps or barriers in the surface potential. Thus 0.1-mil etching between metal electrodes is desirable but is a non-standard process. Furthermore, if the oxide in these gaps is exposed to the ambient air, the surface potential in the gaps is largely uncontrolled, and CCD operation can be adversely affected. Single-level metal

devices will, therefore, require some type of overcoat or resistive sea layer over the gap regions to control and stabilize the surface potential there. Another disadvantage of any three-phase system is a topological one. To contact the three-phase electrodes at least one cross-over or dig-down structure is needed at each stage.

The main advantage of the three-phase single-metal CCD is that it can be made with the minimum number of processing steps. The price for this is the definition of 2 to 3-μm gaps between the gates. Also, the best and more reproducible transfer efficiency has been obtained up to now with closely spaced CCD's in the form of polysilicon gates overlapped by aluminum gates, which are described in the next section.

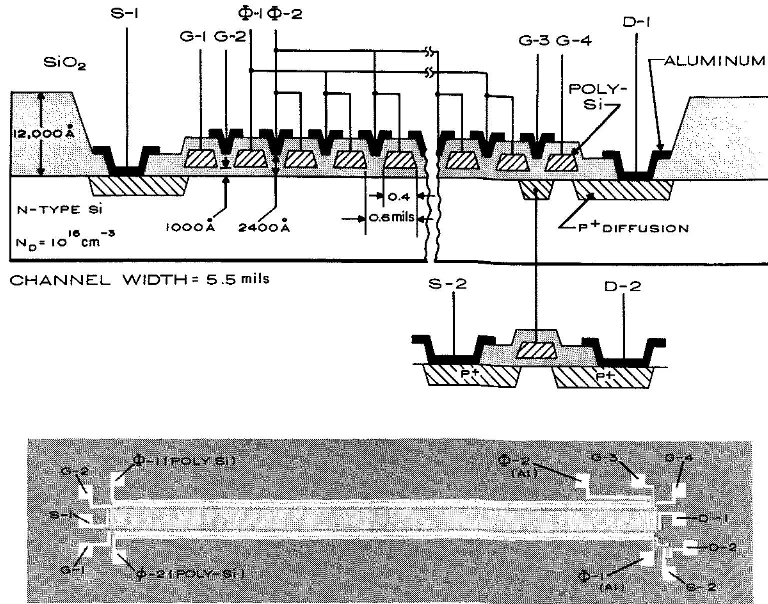

Fig. 5—Cross-sectional view and labeled photograph of CCD-T 128-stage shift register.

Two-phase CCD's

In three-phase CCD's the potential wells are symmetrical, and the directionality of charge flow is maintained by the asymmetry of the clocking voltages as seen in Fig. 2. However, if each potential well had a built-in asymmetry to determine the direction of charge flow, then a symmetrical two-phase clocking scheme could be used to drive the device. The potential well asymmetry required is that the well must be deeper in the direction of charge transfer. This can be achieved by having two thicknesses of oxide under one electrode or by having a variation in substrate doping [See Eq. 1]. A two-phase device has clear topological advantages over a three-phase device since no dig-downs are required for access to the electrodes.

A particularly advantageous method of constructing two-phase CCD's which results in two thicknesses of oxide to provide signal directionality consists of polysilicon gates overlapped by aluminum gates. The method of making these devices is shown in Fig. 4. After definition, the polysilicon gates are partially oxidized to form an insulating layer and to increase the oxide thickness in the region between the gates. The aluminum is deposited and defined so that it overlaps the polysilicon gates as shown. The spacing between electrodes is determined by the polysilicon oxide thickness—typically 2000Å. No gaps are exposed to ambient and standard alignment (0.1 mil) and etching (0.2 mil) techniques result in 1.2 mil per stage (two polysilicon gates and two aluminum gates) spacing. Such devices have been built and experimental results have been obtained.

Experimental results

A variety of CCD device structures have been fabricated at RCA Laboratories in the past two years, including three-phase single-level metal p- and n-channel devices and two-phase polysilicon overlapped by aluminum devices. The two-phase devices have generally been more well behaved and predictable than the single-level metal devices, probably because of the absence of gaps in the two-phase structures.

The crossectional view of a 128-stage two-phase CCD is shown in Fig. 5. In

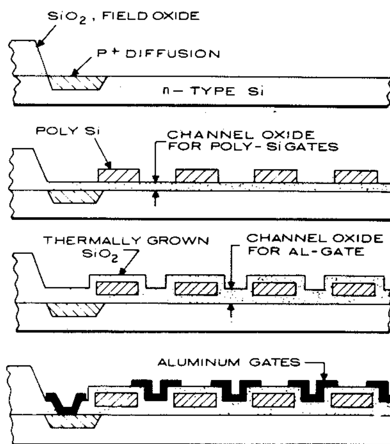

Fig. 4—Construction of the experimental charge-coupled devices.

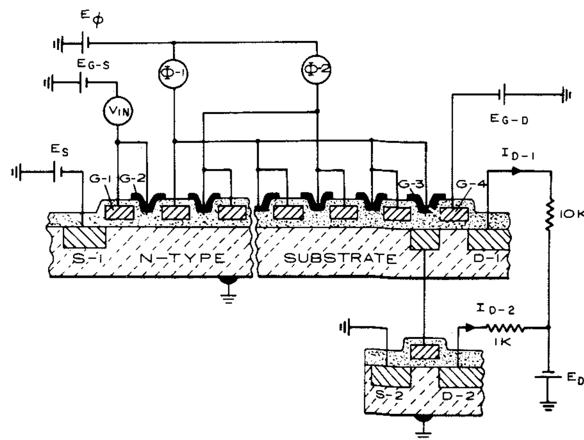

Fig. 6—Circuit diagram for the tests of two-phase charge-coupled shift registers.

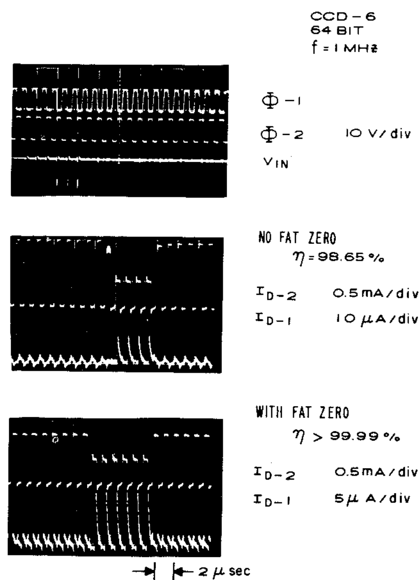

Fig. 7—Typical waveforms for CCD-6 64-stage shift register at 1 MHz.

the operation of this shift register (Fig. 6) the input charge signal is introduced by input pulses V_{in} and the bias voltages E_S and E_{G-S}. The output is detected either directly by "current sensing" as I_{D-1} current or as I_{D-2} by "voltage" or rather "charge-sensing" in which case the potential of a floating diffusion controls the gate of a MOSFET amplifier.

Fig. 7 shows typical oscilloscope waveforms for a 64-stage, two-phase device on a (111) substrate. The improved operation is clearly evident when fat zero is introduced. The experimental measurements of transfer efficiency *vs.* frequency on the two-phase devices have confirmed many of the analytical predictions discussed earlier, especially concerning the transfer of free charge by thermal diffusion and losses due to fast interface states. Fig. 8 shows the

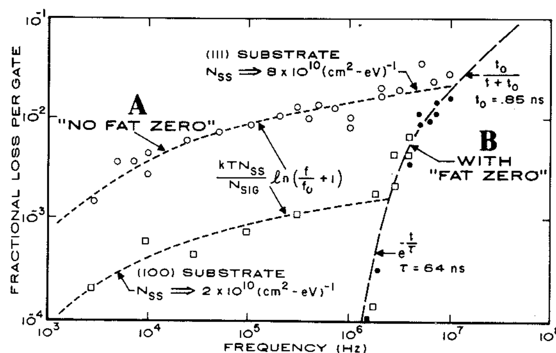

Fig. 8—Fractional loss per transfer *vs.* frequency for 128-stage shift register with and without fat zero.

fractional loss per transfer *vs.* frequency for a 128 stage, two-phase p-channel device with a 10-μm-long polysilicon gate. First, the two left branches of the curve show the loss *vs.* frequency when no fat zero is introduced and fast state losses are expected to dominate. The top curve is for a device built on (111) silicon substrates with expected N_{SS} values of approximately 10^{11} $(cm^2-eV)^{-1}$, and the bottom one is for (100) material with fast state densities expected to be $\sim 10^{10} (cm^2-eV)^{-1}$. A fit of the data to Eq. 7 yields a value of 8×10^{10} for the (111) device and 2×10^{10} for the (100) device, close to the values expected. The $n_{s,o}$ values deduced from the plots were consistent with those expected for thermal generation.

The right branch of the data in Fig. 8 shows the measured loss when a fat zero (10 to 20% of a full well) was intentionally introduced. The fast state losses have been reduced to an immeasurably low level and CCD operation is limited at the higher frequencies by free charge transfer. The doping of the substrate here is $10^{16}cm^{-3}$—too high for fringing fields to be appreciable. Thus, the free-charge transfer is dominated by thermal diffusion. The dotted line shows the loss expected for a 10-μm-gate device—indicating excellent agreement with the actual results. A hole mobility of 250 $cm^2-(V-sec)^{-1}$ was assumed.

Analog signal processing

Charge-coupled devices represent a new LSI technique for the processing of analog information. With charge-transfer loss (inefficiency) $\varepsilon=10^{-4}$ per stage, a figure which has been demonstrated experimentally (as discussed earlier), the analog signal can be transferred through up to 1000 stages of CCD with only minor amplitude and phase degradation which should be acceptable for most applications. One can see, therefore, delay lines for video and audio signals which can be operated with fixed or electronically-variable time delay as one of the direct and obvious applications of CCD's. The time delay, τ_d, for a CCD delay line is

$$\tau_d = N(1/f_c) = N/(2\Delta B) \qquad (8)$$

where N is the number of stages, f_c is the clock frequency, and ΔB is the bandwidth. The CCD delay line operates by sampling the input signal once every clock cycle. Therefore, it is capable of signal bandwidth, ΔB, of close to $f_c/2$. The electronically variable delay is obtained by varying the clock frequency. The maximum time delay, $\tau_d max$, for a CCD delay line is independent of the number of stages and is limited by the dark current generation rate. The practical upper limit for $\tau_d max$ at room temperature is 0.1 to 1.0 s. For example, audio delay of 10 to 20 ms with ΔB of 20 kHz (hi-fidelity delay for quadrasonic speaker synchronization) would require f_c=4 kHz and N=400 to 800 stages.

Since CCD's can store and transfer analog signals under the control of externally applied clock pulses, they can be used as basic components for sorting, switching, and processing of analog information. Examples of such applications are serial-to-parallel and parallel-to-serial conversion, time synchronization and time conversion (compression or expansion), and transversal filters. For example, parallel-to-serial conversion of N elements can be obtained by simultaneous parallel loading of a CCD shift-register by N input circuits. Once the shift-register is loaded, the clock is actuated and the N elements are readout serially at the CCD output. Time conversion can be achieved using a CCD shift register by reading in data at one clock rate and reading out at another higher (compression) or lower (expansion) clock rate. The transversal filters can be used to implement a large class of transfer functions, for example, matched filters. The operation of the transversal filter consists of weighting and summing of parallel signals tapped from various points along the analog delay line.

Charge-coupled image sensor applications

The CCD concept has introduced a revolutionary new approach to the design of self-scanned solid-state image sensors. We will refer to such a device as a charge-coupled imager (CCI). One can think of the CCD as the semiconductor equivalent of an electron-beam tube in which the charge signal can be moved (transferred) and *stored* under the control of the clock voltage pulses free of pick-up and switching transient. The only limitations on the charge-coupling process comes about because the charge transfer is not

100% complete. The finite transfer loss (inefficiency) results in some distortion of the signal, and introduces transfer noise. As will become apparent from the following description of known CCI arrays, the pick-up from the clock voltages is limited to a single output stage.

Two ways by which the optical signal can be introduced into the CCI are illustrated in Fig. 9. The optical input can be introduced from the top of the substrate through the spaces between non-transparent metal gates (Fig. 9a). Top illumination of the CCI is also possible by transmitting the optical input through transparent gates such as thin polysilicon. An alternate approach (Fig. 9b) consists of thinning the substrate in the optically-sensitive area and applying the optical input from the back side of the substrate. Fig. 9 also illustrates two ways by which the output can be removed from the CCI array. Output-1 is the current output derived from the drain diffusion *D*. The low impedance output-2 samples the voltage of the floating diffusion *F* and is proportional to the charge signal. Let us assume now that an optical input is applied to such a CCD register while the clock voltages are adjusted so that one potential well is created at each stage along the CCD channel. As suggested in Fig. 9a, the photogenerated charge will collect in these wells during the optical integration time. At the end of the integration time, the accumulated charge packets representing the integrated optical input are shifted down the CCI register and detected by a single output amplifier. To prevent smearing of the image, the optical integration time should be much larger than the total time required to transfer the detected image from the CCD line sensor. Since all charge elements are amplified by the same amplifier, non-uniformities—usually a problem in optical arrays in which each sensor elements uses a separate amplifier—are avoided. Since there is no direct coupling of the clock voltages to the charge signal in the CCD channel, the clock pick-up is limited only to a single output stage. In addition, since only the clock frequency, which is outside of the video bandpass, is used in CCD transfer, clock pick-up is not the problem as it is in *x-y* scanned arrays where one of the clocks occurs at the horizontal line frequency and cannot be removed by appropriate filtering.

A more effective CCD line sensor (or CCI line array) is shown schematically in Fig. 10a. Here, the optical input can be continuously integrated by the linear array of photodiodes. During the operation, the detected line image is periodically transferred in parallel to the CCD register from where it is read-out serially. It is essentially an analog parallel-to-series converter, with time-integrated optical input and electrical output. A dual CCD-channel line-sensor is shown in Fig. 10b. The operation of this CCI is the same as for the line sensor described above except that the detected image is transferred into two parallel CCD registers and then combined into a single output line. The advantage of the dual CCD-channel line-sensor over the line-sensor shown in Fig. 10a is double resolution.

One way of implementing an area CCI is illustrated in Fig. 11. This array can be visualized as a parallel array of the previously described linear arrays whose outputs are transferred in parallel into a single output register. The operation of this CCI is as follows. Once every frame time the charge signal detected by the photodiode array is transferred into the vertical CCD channels, which are not photosensitive. Then, the entire detected image is shifted down in unison by clock A and transferred into the output register one (horizontal) line at a time. The horizontal lines are then transferred out from the output register by the high frequency clock B before the next horizontal line is shifted in.

Another frame transfer CCI that does not require separate photosensors is shown in Fig. 12.[13-16] In this CCI, the photosensor function is performed by an additional photosensitive CCD array. This system is composed of three functional parts: the photosensitive array, temporary storage array, and the output register. The optical image is detected by the photosensitive array. Then assuming a TV format with 1/60-s frame time, the detected image is transferred into the temporary storage array by clocks A and B, during the vertical blanking time, (900 μs). From there, it is shifted down one horizon-

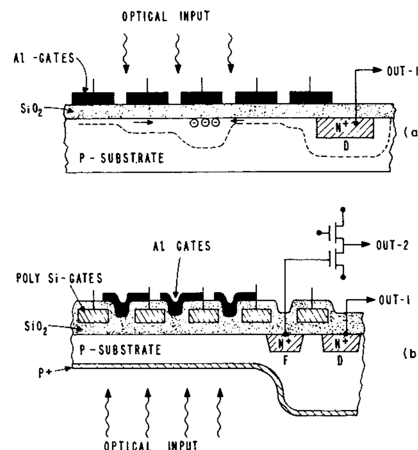

Fig. 9—Crossectional view of (a) top (front) illuminated CCI; (b) back illuminated CCI

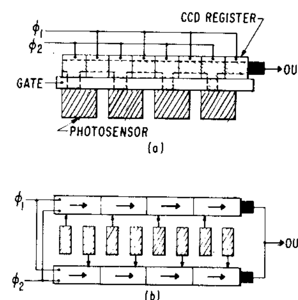

Fig. 10—Charge-coupled line sensors: (a) with single CCD channel; (b) with two parallel CCD channels.

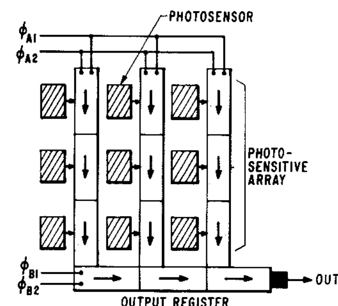

Fig. 11—Frame transfer with separated photosensors.

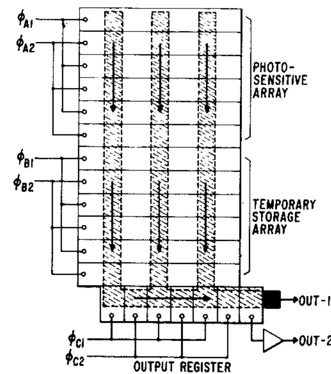

Fig. 12—Frame transfer CCI with a temporary storage array.

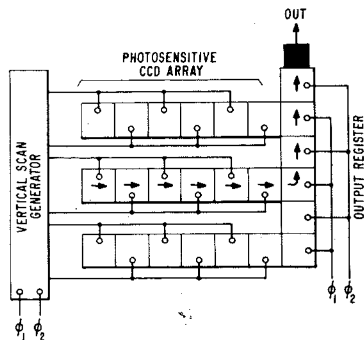

Fig. 13—Horizontal line-by-line transfer CCI.

tal line at a time into the output register and transferred out by the high speed clock C. The time available for parallel loading of the output register corresponds to the horizontal line retrace time of 10 μs, which leaves 50 μs for the read-out of the horizontal line from the output register.

A third type of CCD area array (Fig. 13) was made originally at RCA Laboratories using bucket-brigade shift registers.[17-19] This system consists of parallel array of photosensitive, horizontal, CCD channels, all leading into a single output register. This CCI operates by transferring, under the control of the vertical clock generator, one horizontal line at a time, from the photosensitive CCD array to the output register and out.

The frame-transfer system with temporary storage array has been chosen for the development of a two-phase CCI TV camera. Although this system requires somewhat larger area of silicon than the other two systems, it can be designed with known CCD techniques. Using design rules applied to our existing two-phase CCD, this system can be implemented with optical resolution elements on 1.2-mil centers. A device with blooming control and an electronically variable exposure time can be constructed more easily with the frame transfer system. However, unlike the charge-transfer system with separate photodiode arrays, it requires back-side illumination for efficient operation.

In addition to the advantages of solid-state construction offering small size, rugged construction, long life, and low power dissipation, CCI TV cameras should be relatively low-noise sensors —about an order of magnitude more sensitive than the silicon vidicon. While the sensitivity of the silicon vidicon is limited by the output capacitance (10 to 20pF), the output capacitance of a CCI can be about two orders of magnitude smaller, 0.1 pF. Analysis shows[20] that the sensitivity of the CCI designed with the output amplifier integrated on the same chip should be limited by the transfer noise associated with the charge trapped by the fast interface states in the surface channel CCD, and the shot noise due to the background charge either thermally generated as the dark current, or introduced as a "fat zero" to eliminate the interface state losses.

Digital storage applications

One of the potentially attractive digital applications of the CCD is an inexpensive bulk digital storage. However, unlike the case of analog processing and image sensing devices where the CCD offers a new technology previously not available, the CCD must now compete in price and performance with other storage devices. Using comparable layout rules, the CCD offers packing density advantages only about 2 to 4 over the dynamic MOS memories.[21] However, except for the signal regeneration and input/output stages, the CCD memories can be made without diffusions and contact openings. This implies that eventually CCD memories can be made with much higher packing density as well as higher yield and larger chip sizes than will be possible using MOS circuits.

Charge-coupled shift registers are basically analog devices with no signal gain mechanisms. To use these devices for storage of digital signals, it is necessary to periodically refresh or to regenerate the charge signal. Simple charge regeneration, such as shown in Fig. 14, can be laid-out in an area no larger than the area required for 2 to 4 stages of shift register.[7]

Various system organizations can be considered for the construction of charge-coupled memories. The choice of the system organization depends on the desired system performance. Two types of systems in the form of a single large-storage loop per chip are illustrated in Fig. 15. As is shown, the signal flow in system A follows a serpentine pattern and has signal refreshing stages at each corner. The system B on the other hand is in the form of two serial and one large parallel shift register as well as a single signal re-

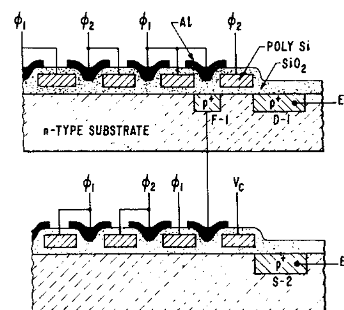

Fig. 14—Schematic cross-section of two CCD shift registers with simple charge regeneration scheme using a floating diffusion.

generation, similar to the frame transfer CCI shown in Fig. 12. Two-phase charge-coupled structures are needed for an efficient design of system A. The system B on the other hand could be constructed with either two-phase or three-phase structures. At this point, it should also be noted that the frame-transfer CCI with a separate store can be designed so that it can also be operated as a digital store, or as an electronic camera for digital images.

The system organizations for obtaining more parallel operation, smaller storage loops, and shorter access time are shown in Fig. 16. The addressing of the individual storage loops in system C is accomplished by a decoder. Still more parallel organization with smaller storage loops addressable by an x-y matrix switch is illustrated by system D. As in the case of system A, two-phase or uniphase charge-coupled devices will also lead to a more efficient design of systems C and D.

Finally, the most parallel memory is system E, shown in Fig. 17. This system represents the charge-coupled version of one transistor-per-bit refreshable memory. The signal is stored in single charge-coupled elements that are periodically gated by the word lines into the digit-line diffusions. Each digit-line drives a signal-regeneration or sense amplifier whose output regenerates the information in the selected bit location and also may be gated-out. The main difference is that, in systems A through D, the signal-regeneration amplifiers are driven by high impedance charge-coupled storage loops. Thus, high packing density can be accomplished since relatively high voltage (on the order of several volts) is available at the low capacitance input of the signal regeneration for small charge signals representing the information. However, system E

has a large number of individual charge-storage elements connected in parallel to a single regeneration amplifier. Therefore, the input voltage available to the sense amplifier is attenuated by the capacitance divider corresponding to a relatively small storage capacitance and a considerably larger capacitance associated with digit-line amplifier input.

Our analysis of the transfer of the free charge indicates that the maximum bit rate for such serial memories may be in excess of 10^7 bits/s. The chip selection and other signal switching may, however, impose a practical upper limit on the bit rate in the range between 10^6 to 10^7 bits/s. Assuming a packing density of about 1 square mil of silicon per bit of storage, the charge-coupled serial memories may be constructed with about 40 kilobits on a single chip of silicon having dimensions of about 200×200 mils. The above packing density involves more or less state-of-the-art circuit layout rules. Therefore, considerably higher packing density may be achieved by employing high resolution processing.

Another attractive feature for a large-capacity charge-coupled serial memory is a rather low power requirement if the high-frequency phase-voltage pulses are applied only to the selected shift registers while the unselected storage loops are idling at a much lower clock rate. Assuming a channel oxide of 2000Å and an area of one charge-coupled electrode of 10^{-6}cm², the corresponding capacitance of each phase electrode is about 1.76×10^{-14} F. For the phase voltage of 10V, the reactive energy per phase for one bit storage is about 2×10^{-12} J. For a clock rate of 10^7 bit/s, the reactive power is estimated as 20 μW per bit. If we assume that for a 10^8-bit memory no more than 10^5 bits are operating at any time at the rate of 10^7 bits/s, the clock power required for the selected chips will be 2W. The total standby power for the 10^8-bit memory will also be 2W if the idling clock rate for the unselected chips is chosen as 10^4 bits/s.

Conclusions

Although the CCD concept is not quite three years old, the operation of these devices is quite well understood, and has been experimentally verified. Charge transfer efficiencies of 99.99% have been achieved. A number of applications in the area of analog signal processing, image sensors, and digital memories are in the process of development. Some examples of CCD products that may soon become commerically available using present LSI technology are electronically-variable analog delay lines and low-resolution image sensors (100×100 elements). It is expected that the development of a full resolution CCI TV camera (500×500 elements) should provide the impetus for the achievement of a "giant" chip LSI technology.

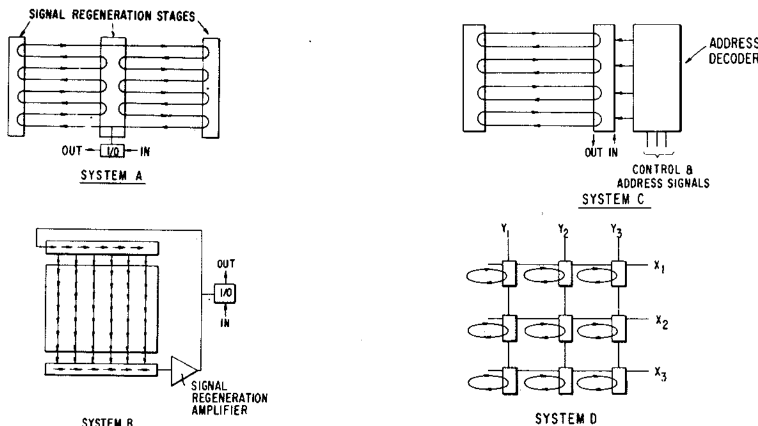

Fig. 15—Two types of memory systems using single storage loop.

Fig. 16—Two memory system organizations for obtaining more parallel operation, smaller storage loops, and shorter access times.

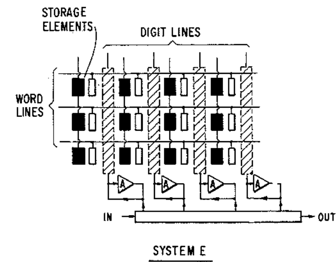

Fig. 17—Charge-coupled version of one transistor-per-bit refreshable random access memory.

References

1. Boyle, W. S. and Smith, G. E., "Charge-Coupled Semiconductor Devices," *Bell System Tech. J.* (1970) p. 587.
2. Amelio, G. F.: Tompsett, M. F.; and Smith, G. E., "Experimental Verification of the Charge-Coupled Device Concept," *Bell System. Tech. J., Briefs* (April 1970) p. 593.
3. Tompsett, M. F., and Zimany, E. J., "Use of Charge-Coupled Devices for Analog Delay," *Digest of Technical Papers,* 1972 IEEE International Solid-State Circuits Conference, Philadelphia (Feb. 1972) p. 136.
4. Kosonocky, W. F. and Carnes, J. E., "Two-Phase Charge-Coupled Shift Registers," *Digest of Technical Papers,* IEEE International Solid State Circuits Conference, Philadelphia, Pa. (Feb. 1972) p. 132.
5. Kosonocky, W. F. and Carnes, J. E., "Two-Phase Charge-Coupled Device," *Final Report PRRL-72-CR-6,* Langley Research Center, Hampton, Virginia, NASA, Contract No. NAS 1-10983, (Feb. 1972).
6. Heiman, F. P., "On the Determination of Minority Carrier Lifetime from The Transient Response of an MOS Capacitor," *IEEE Trans. Elect. Dev.* Vol. ED-14, No. 11, (1967) p. 781-786.
7. Kosonocky, W. F. and Carnes, J. E., Charge-Coupled Digital Circuits," *IEEE J. Solid-State Circuits* Vol. SC-6, (1971) p. 314.
8. Carnes, J. E.; Kosonocky, W. F.; and Ramberg, E. G., "Free Charge Transfer in Charge-Coupled Devices," *IEEE Trans. on Electron Devices,* Vol. ED-19, No. 6, (1972) pp. 798-808.
9. Carnes, J. E. and Kosonocky, W. F., "Fast Interface State Losses in Charge-Coupled Devices," *Appl. Phys. Ltrs.* Vol. 20, No. 7 (April 1, 1972) p. 261.
10. Engeler, W. E.; Tiemann, J. J.; and Baertsch, R. D., "Surface Charge Transport in Silicon," *Appl. Phys. Letters* 17, (1970) p. 469.
11. Kim, C. K., and Lenzlinger, M., "Charge Transfer in Charge-Coupled Devices," *J. Appl. Phys.* 42, (1971) p. 3586.
12. Carnes, J. E.; Kosonocky, W. F.; and Ramberg, E. G., "Drift-Aiding Fringing Fields in Charge-Coupled Devices," *IEEE J. Solid State Circuits* SC-6, (1971) p. 322.
13. Bertram, W. J., "Application of Charge-Coupled Device Concept to Solid State Image Sensors," *Digest of Technical Papers,* 1971 IEEE International Convention, New York (March 22-25, 1971) p. 250.
14. Tompsett, M. F.; Amelio, G. F.; Bertram, W. J.; Buckley, R. R.; McNamara, W. J.; Mikkelsen, J. C.; and Sealer, D. A., "Charge Coupled Imaging Devices: Experimental Results," *IEEE Trans. Electron Devices,* ED-18, (Nov. 1971) p. 992.
15. Bertram, W. J.; Sealer, D. A.; Sequin, C. H.; Tompsett, M. F.; Buckley, R. R., "Recent Advances in Charge-Coupled Imaging Devices," Digest of Technical Papers," 1972 IEEE International Convention, New York (March 20-23, 1972) p. 292.
16. Weimer, P. K.; Kovac, M. G.; Pike, W. S.; Shallcross, I. V., "Charge-Coupled Imager," *Final Report,* Sept. 1972, Contract Number 0014-71-C-0415.
17. Kovac, M. G.; Weimer, P. K.; Shallcross, F. V.; and Pike, W. S., "Self-Scanned Image Sensors Based Upon Bucket-Brigade Scanning," abstract of paper presented at the IEEE Electron Devices Meeting, Washington, D. C., (Oct. 1972).
18. Kovac, M. G.; Shallcross, F. V.; Pike, W. S.; and Weimer, P. K., "Image Sensors Based on Charge Transfer by Integrated Bucket Brigades," International Electron Devices Meeting, Washington, D. C., (Oct. 11-13, 1971).
19. Kovac, M. G.; Pike, W. S.; Shallcross, F. V,; and Weimer, P. K., "Solid State Imaging Emerges from Charge Transport," *Electronics,* (Feb. 28, 1972) p. 72.
20. Carnes, J. E. and Kosonocky, W. F., "Noise Sources in Charge-Coupled Devices," *RCA Review,* Vol. 33, No. 2, (June 1972) pp. 327-343.
21. Karp, J. A., Rezitz, W. M.; and Chou, S., "A 4096-Bit Dynamic MOS RAM," *ISSCC Digest of Tech. Papers,* (Feb. 1972) pp. 10-11.